ABSTRACT OF THE INVENTION

The present invention relates to a power socket for a microelectronic device that, in one embodiment, uses a low-resistance power and ground terminal configuration. In another embodiment, a low-resistance power and ground terminal configuration is combined on the power socket with a vertically oriented interdigital capacitor that is used to lower inductance. By this combination a significantly lowered impedance is achieved during operation of the microelectronic device.

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